Active inrush current limiter based on SCRs for 3.6kW bridgeless totem pole PFC

Agenda

- **ST AC-DC inrush current limiter solutions**
- PFC totem pole topology using SiC MOSFETs and thyristors
- Evaluation board performance
- Takeaways

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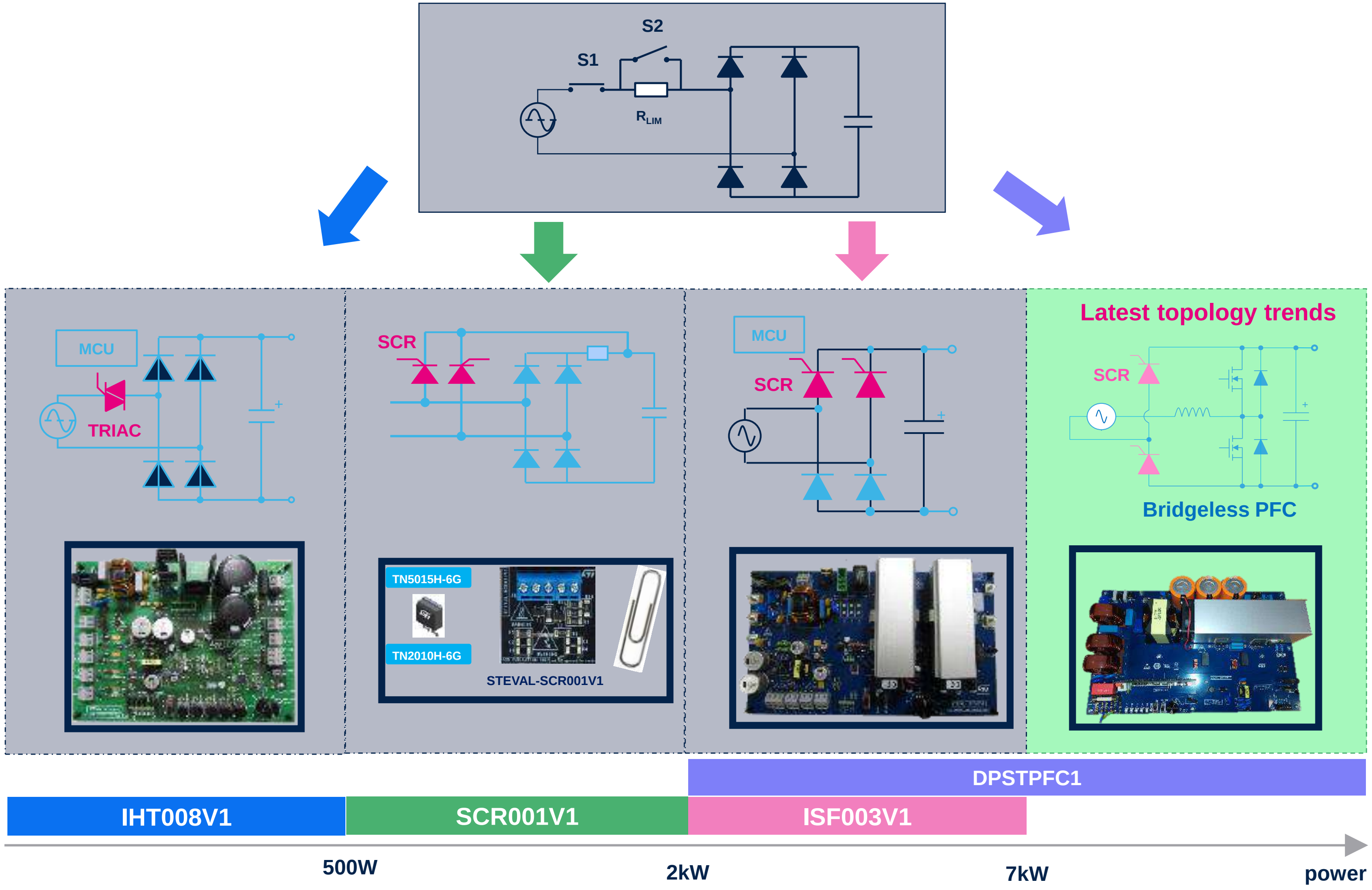
ST AC-DC inrush current limiter solutions



SMART

- Programmable soft power up control
- Controlled multiple peak current limitation
- Zero-current Switch

SAFETY

- No Contact Bounce: no spark, no EMI
- Faster line-drop recovery
- Increase switching life expectancy

COMPACT

Low profile design, smaller height thanks to D²PAK package

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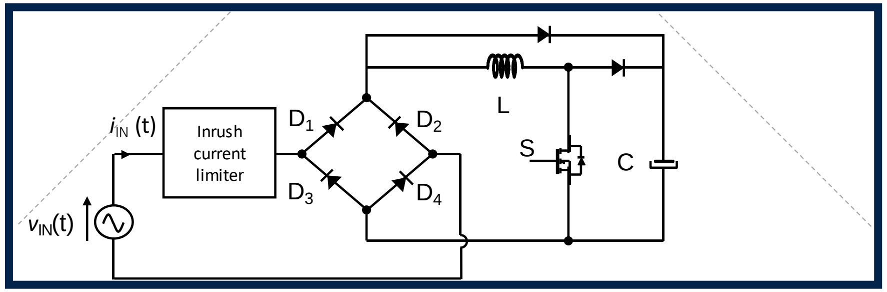
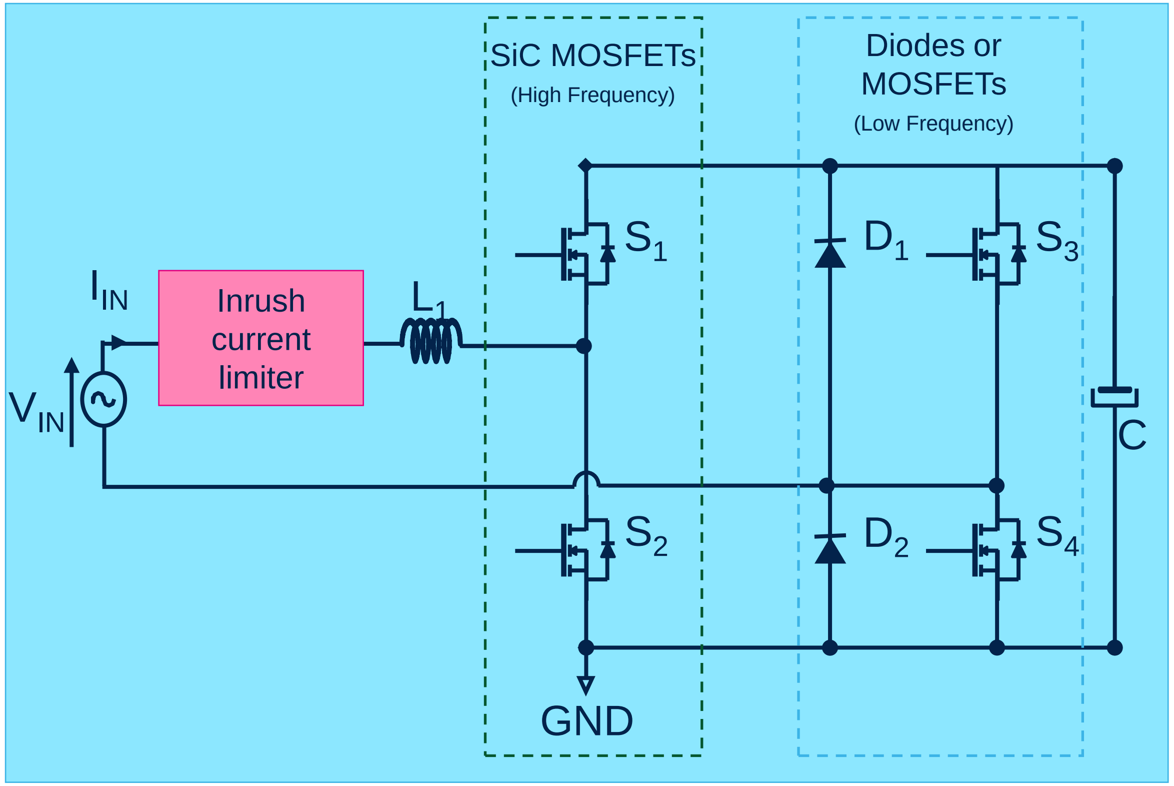
PFC totem pole topology (1/5)
Traditional PFC totem pole

- A conventional PFC circuit:
  - Consists of a full bridge rectifier and a boost pre-regulator
  - A large portion of system losses are in the diode bridge

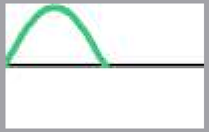


- In a traditional totem pole PFC:
  - The diode losses are eliminated
  - Low frequency switches are diodes or MOSFETs
  - Needs an Inrush current limiter (NTC + relays)

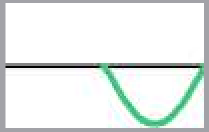


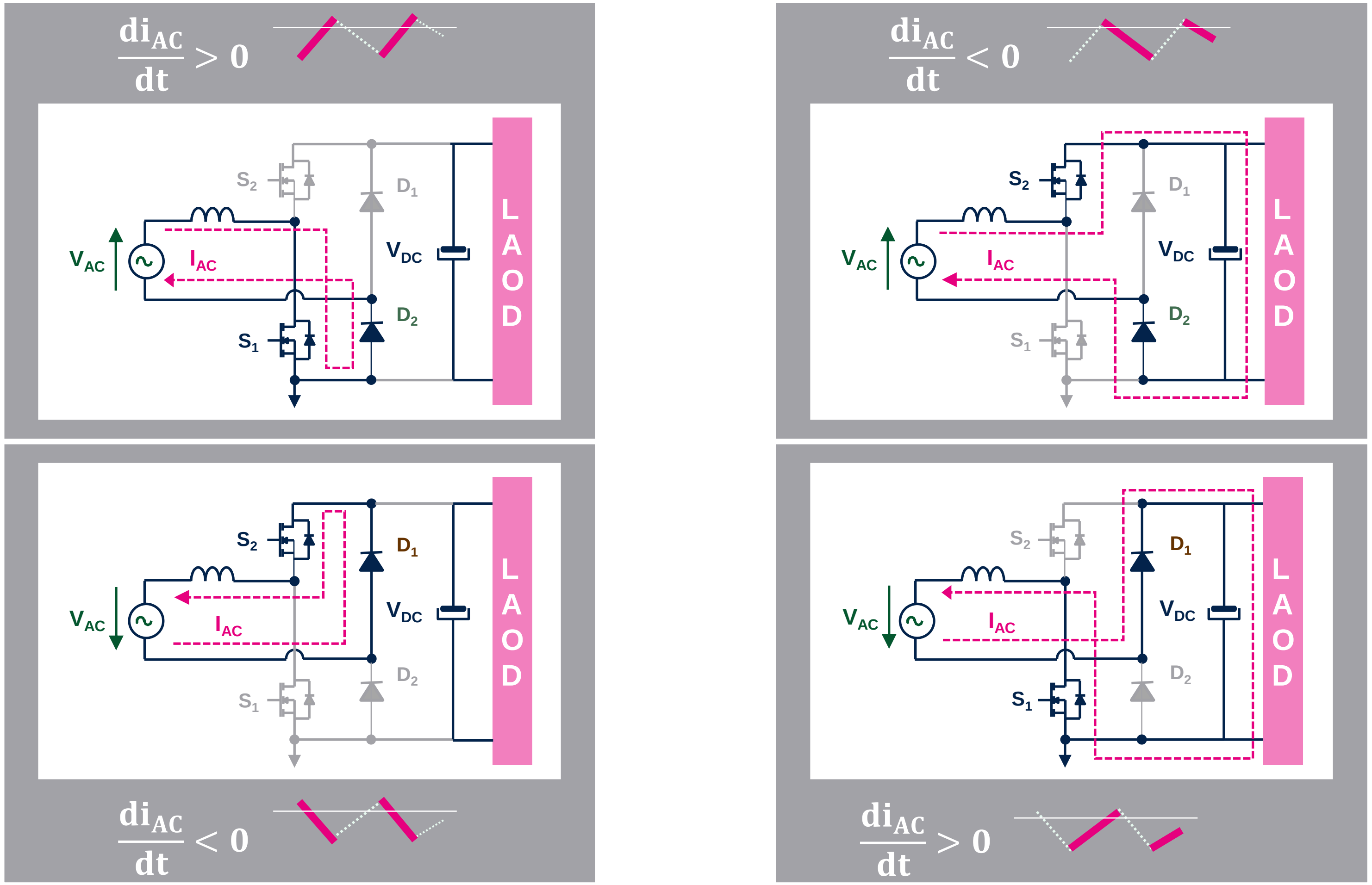
PFC totem pole topology (2/5) Operation

$V_{AC} > 0$



$V_{AC} < 0$





- D1 /D2 diodes (can be replaced by MOSFETs) works at AC line frequency
- Needs an Inrush current limiter (NTC and Relay)

} SCRs solution

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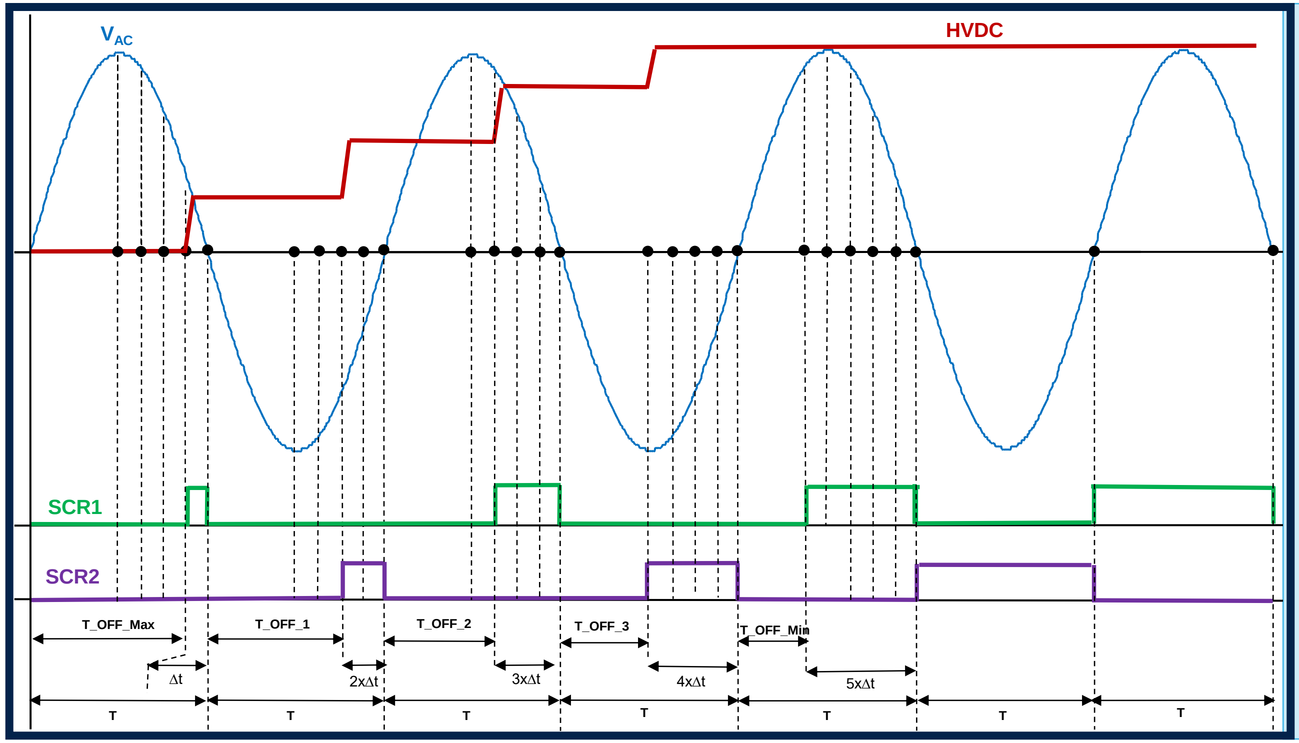
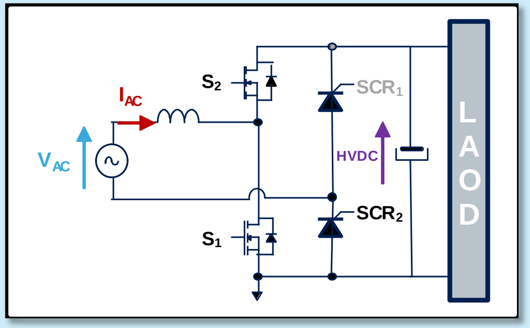
PFC totem pole topology (3/5)
SCRs phase control



- Bulk capacitor is charged according to time-depending pulse train driving SCR1 and SCR2
- SCR1 and SCR2 are synchronized according to the zero crossing (ZVS) of the AC line
- SCR1 and SCR2 are alternatively controlled according to the AC line polarity by reducing the turn-on delay (“T_OFF”) by a constant Δt at each half AC line cycle
- SCR1 and SCR2 are controlled by phase angle up to the turn-on delay (“T_OFF”) is lower than “T_OFF_Min”



- Control the inrush-current to charge a DC bus capacitor
- Disconnect the DC bus capacitor from the AC mains when it does not have to operate

PFC totem pole topology (4/5)
MOSFET vs SCR comparison

As low frequency switching, only the conduction losses are considered

SCR

$$P_{d\_SCR} = \frac{V_{TO} I_{LINE(RMS)} \sqrt{2}}{\pi} + R_d \frac{I^2_{LINE(RMS)}}{2}$$

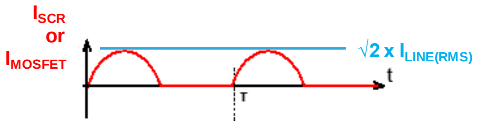
MOSFET

$$P_{d\_MOSFET} = \frac{R_{DS(ON)} I^2_{LINE(RMS)}}{2}$$

Equilibrium for Pd_SCR = Pd_MOSFET:

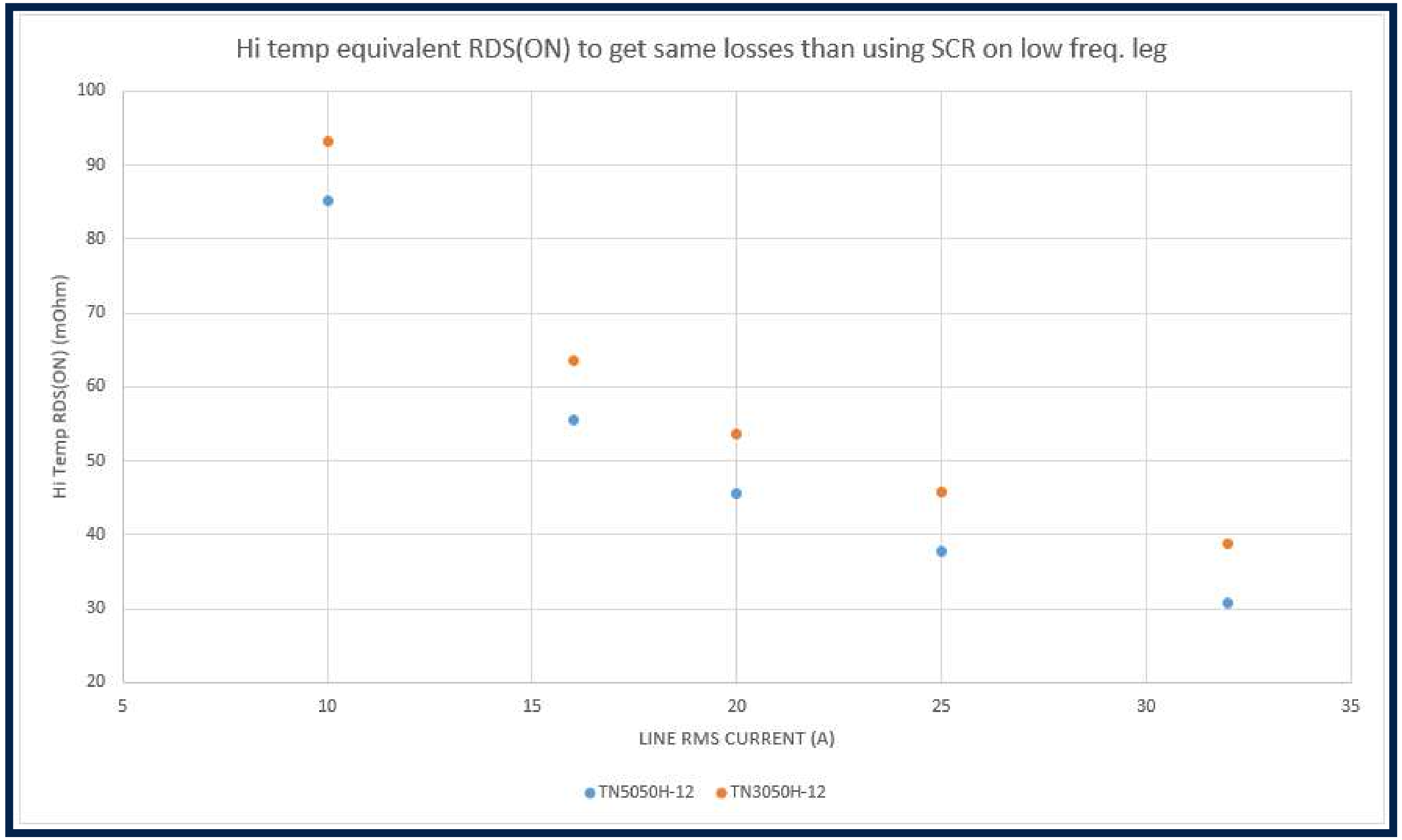
$$R_{DS(ON)} = \frac{2\sqrt{2} V_{TO}}{\pi I_{LINE(RMS)}} + R_d$$

Note: losses are calculated for single half-wave conduction (so for each device).
Multiply by 2 to calculated the total losses (for the 2 SCR or the 2 MOS).



PFC totem pole topology (5/5) MOSFET vs SCR comparison

- SCR have the same efficiency as MOSFET but with a silicon area more optimized
- With the traditional NTC / Relay solution, the contact resistance relay is needed to be into account
- SCRs surge current capabilities makes the SCR the ideal candidate for bridge applications where the devices can be submitted to voltage surges



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Agenda

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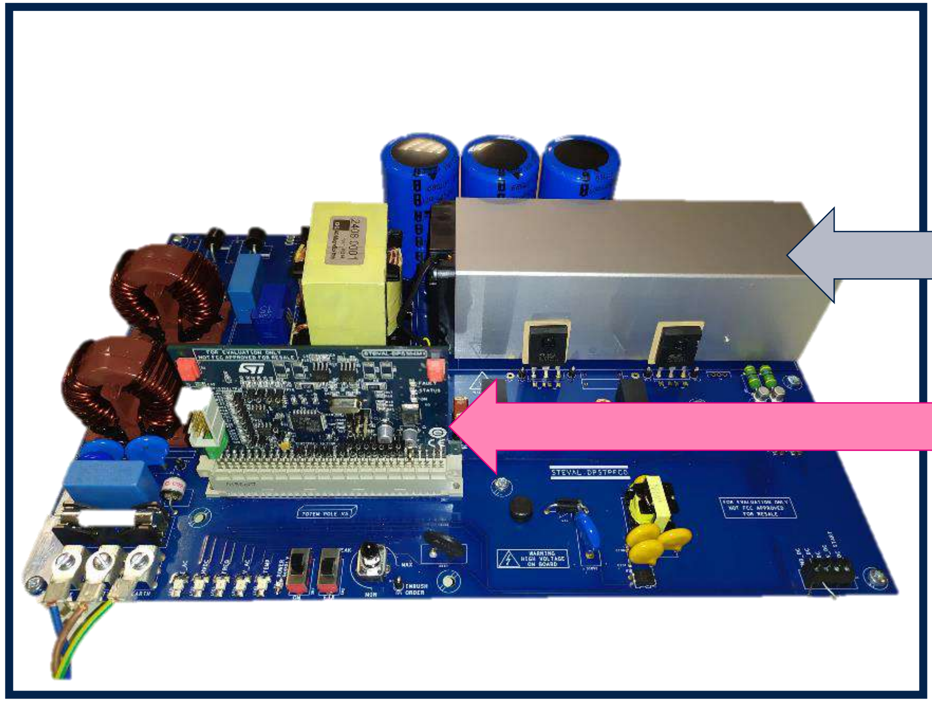
Evaluation board performance
Design content



Reference	Name	Description
STEVAL-DPSTPFC0	AC - DC power board	Bridgeless Totem Pole boost with auxiliary supply
STEVAL-DPS334M1	PFC control board	32-bit MCU control board
STEVAL-DPSADP01	Adapter Board	Interface for MCU debugging and USART communication

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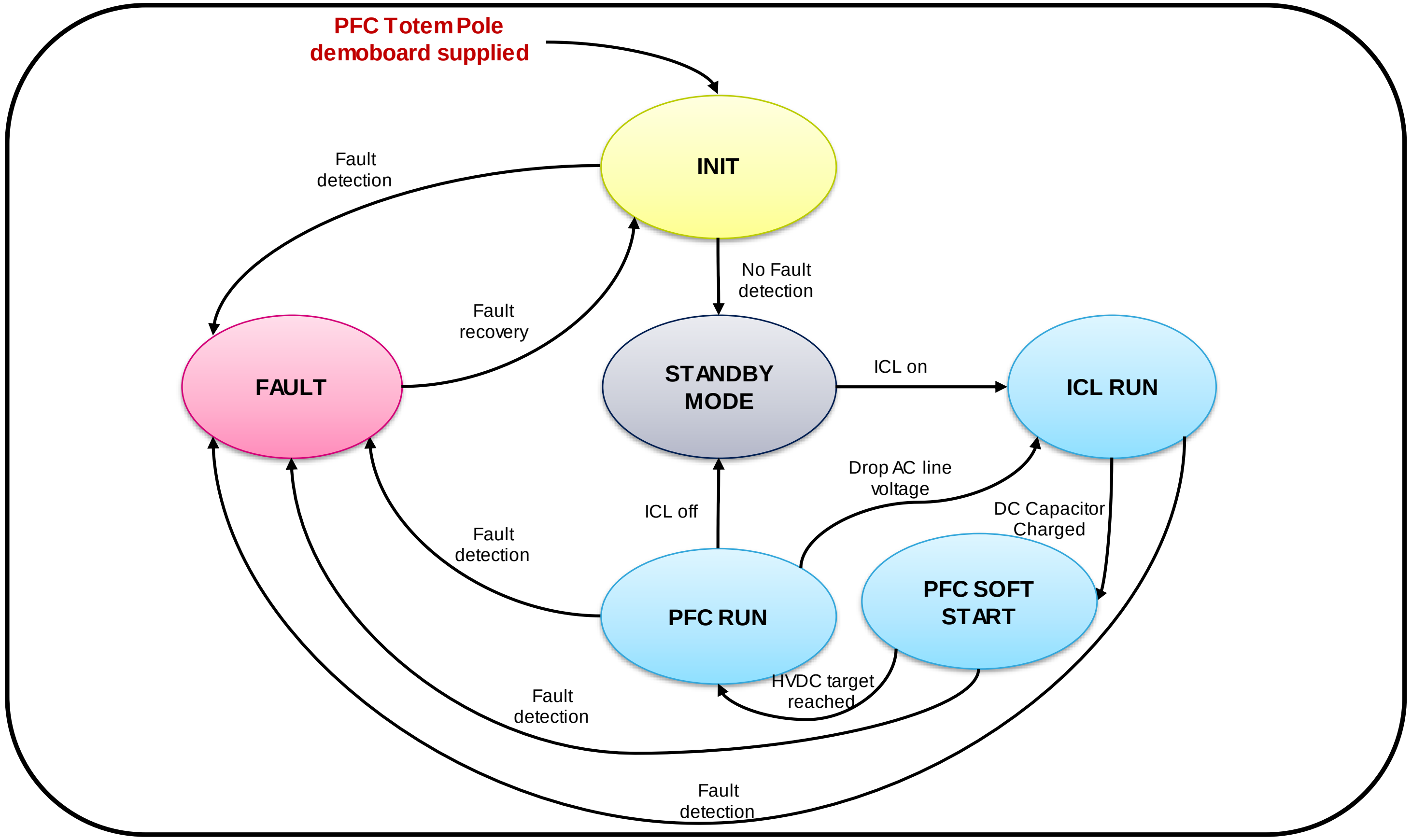
Evaluation board performance Firmware overview



- Control loop:
  - Average current-mode control method I
  - Continuous and discontinuous conduction mode
- Outer voltage loop performed at 72 kHz
- Outer voltage loop performed at 2 times of AC line frequency
- DFF is used to pre-calculate a duty ratio and to improve the transient response
- Digital average current mode control in CCM and DCM including:
  - Bus voltage and AC line currents sampling
  - Voltage error calculation
  - Voltage PI regulation
  - Reference current calculation
  - Current error calculation
  - Duty cycle feed-forward generation
  - Final duty cycle computation

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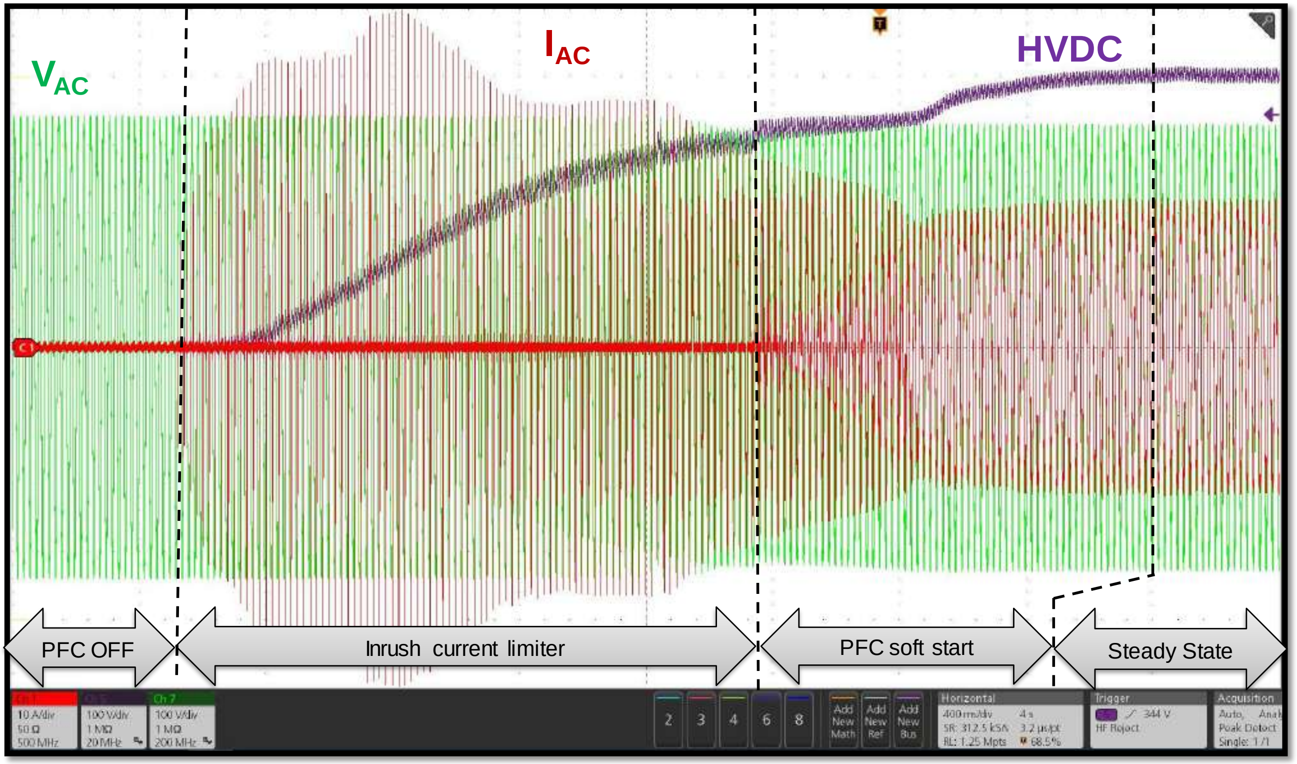
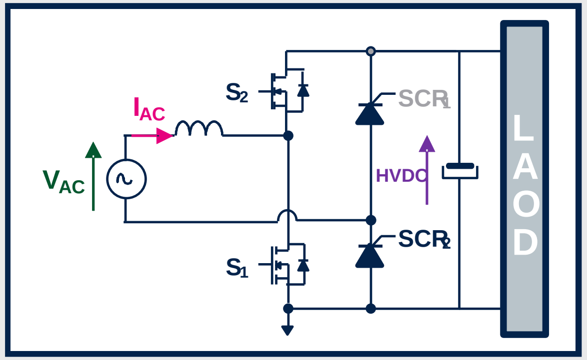
Evaluation board performance
PFC totem pole start-up



To ensure a smooth PFC start-up a soft start routines has been implemented on the MCU firmware:

1) **Inrush current limiter**: SCRs are controlled with a progressive phase control and the output capacitor can be smoothly up to the AC line peak voltage.

2) **PFC soft start**: The output voltage reference is controlled from AC line peak voltage to 400 Vdc with a smoothly voltage ramp.



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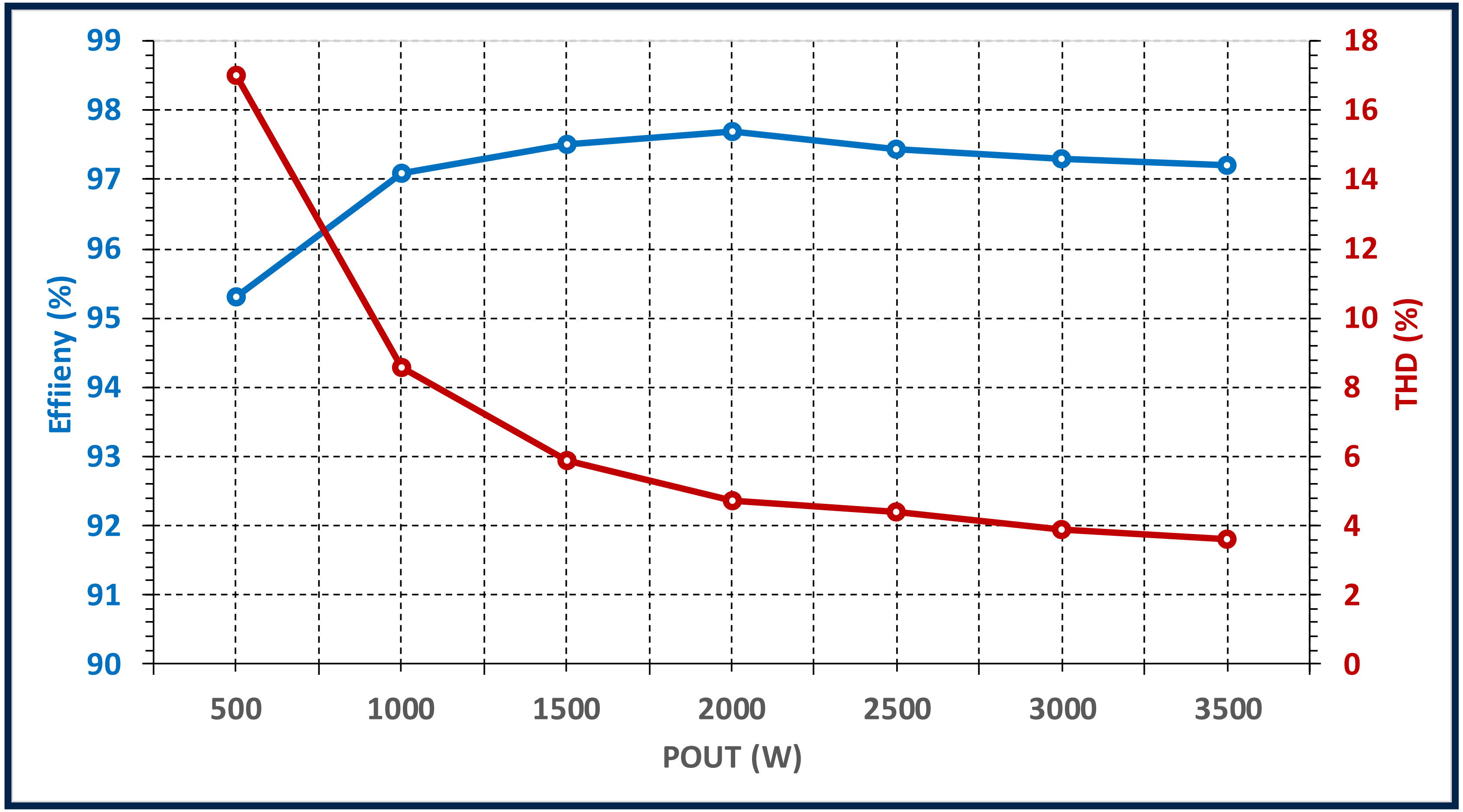
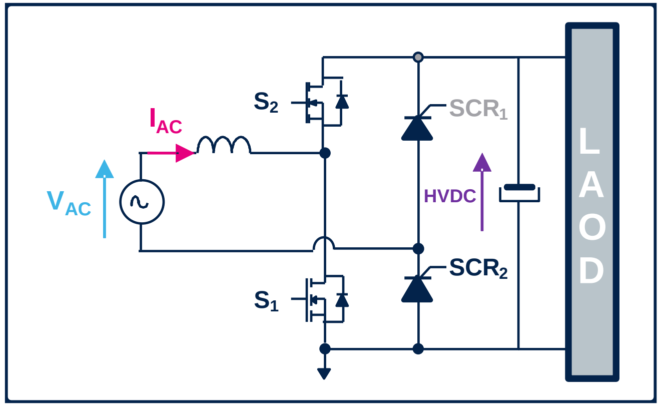
Evaluation board performance
PFC efficiency / THD measurement

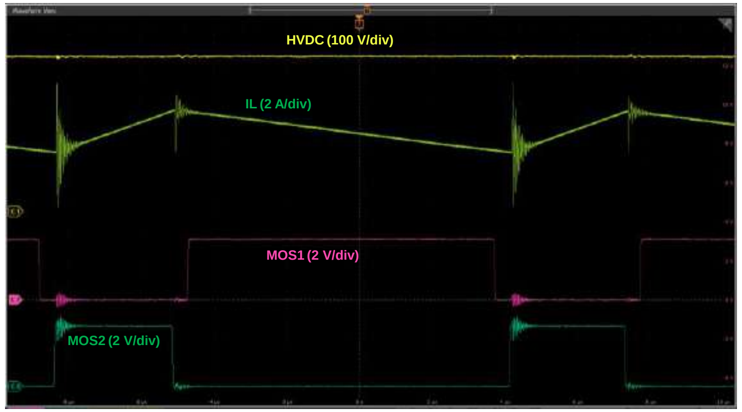
VAC = 230 VRMS @ 50 Hz



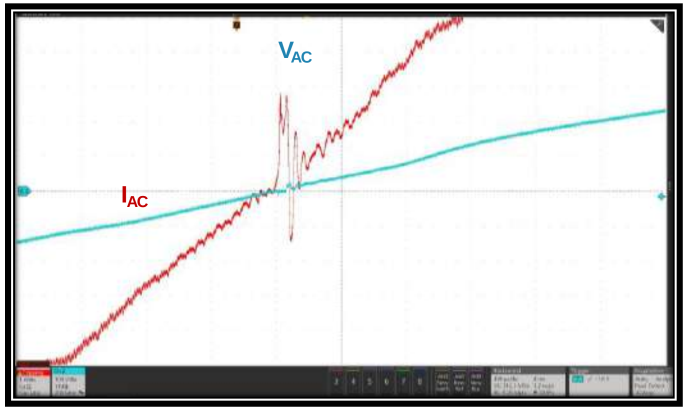
Evaluation board performance
SiC MOSFET control

- SiC MOSFETs are operating in synchronous conduction mode to improve efficiency





- Current spike is generated at each AC line zero cross



- Duty ratio of switch changes abruptly from zero to almost 100% after each AC line zero cross
- High voltage is applied to the inductor (HVDC). A high positive current spike is generated
- Same phenomenon with diode or MOSFET

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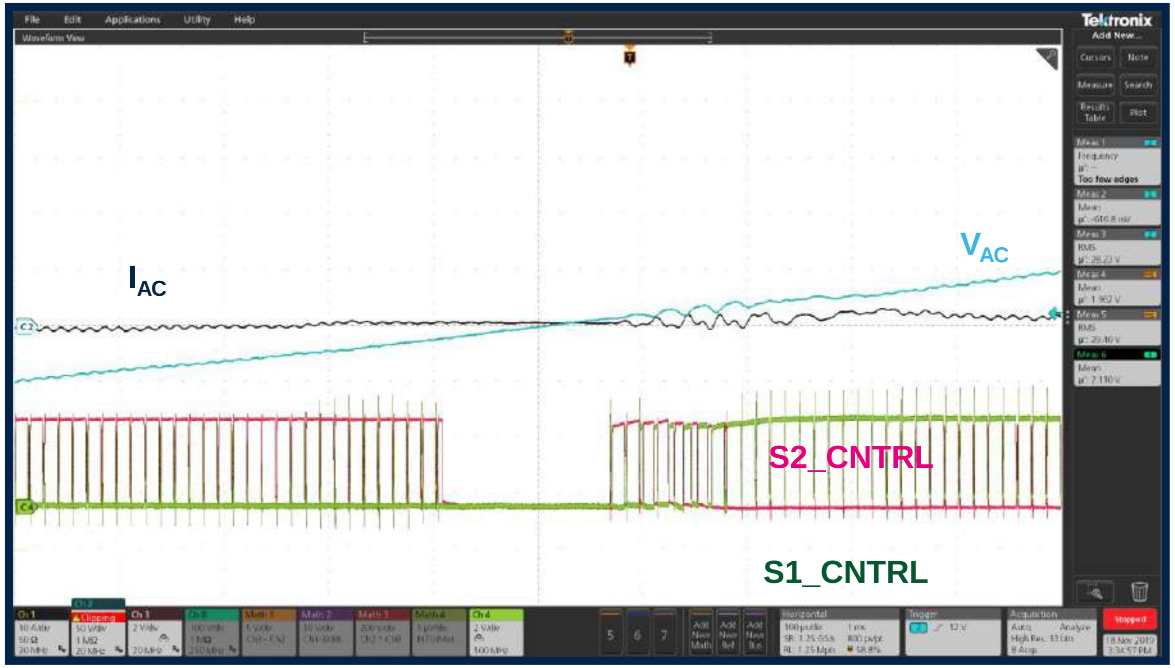
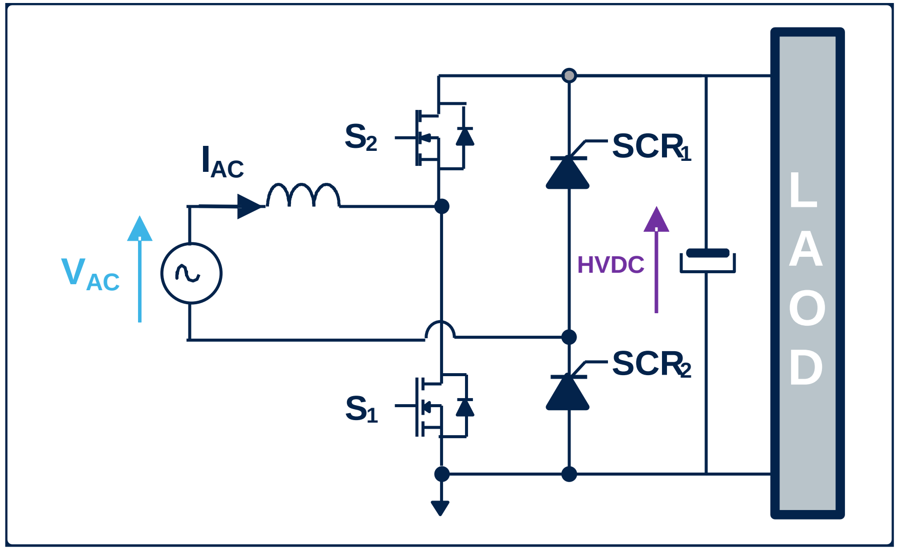
Evaluation board performance
SiC MOSFET control

- SiC MOSFETs are controlled with a smart Duty Cycle control at each AC line zero cross
  - To reduce peak current through boost inductor at the AC line zero crossing
  - To improve common mode noise





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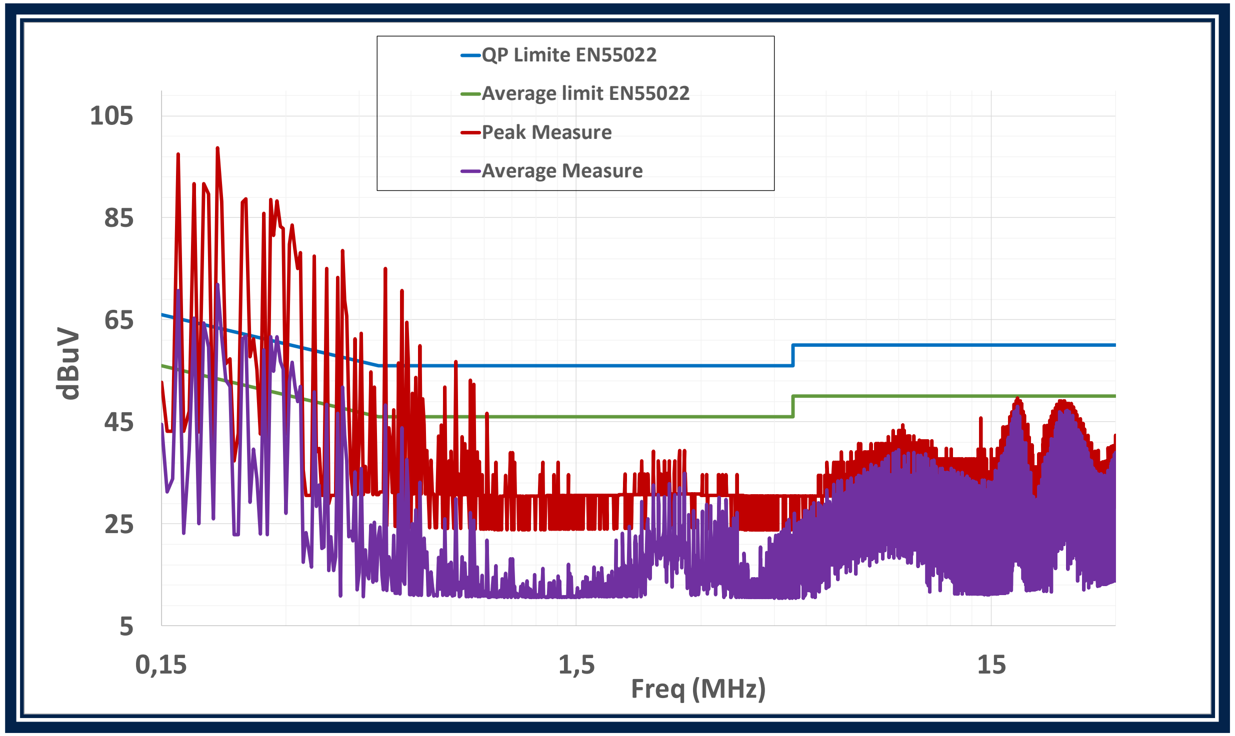
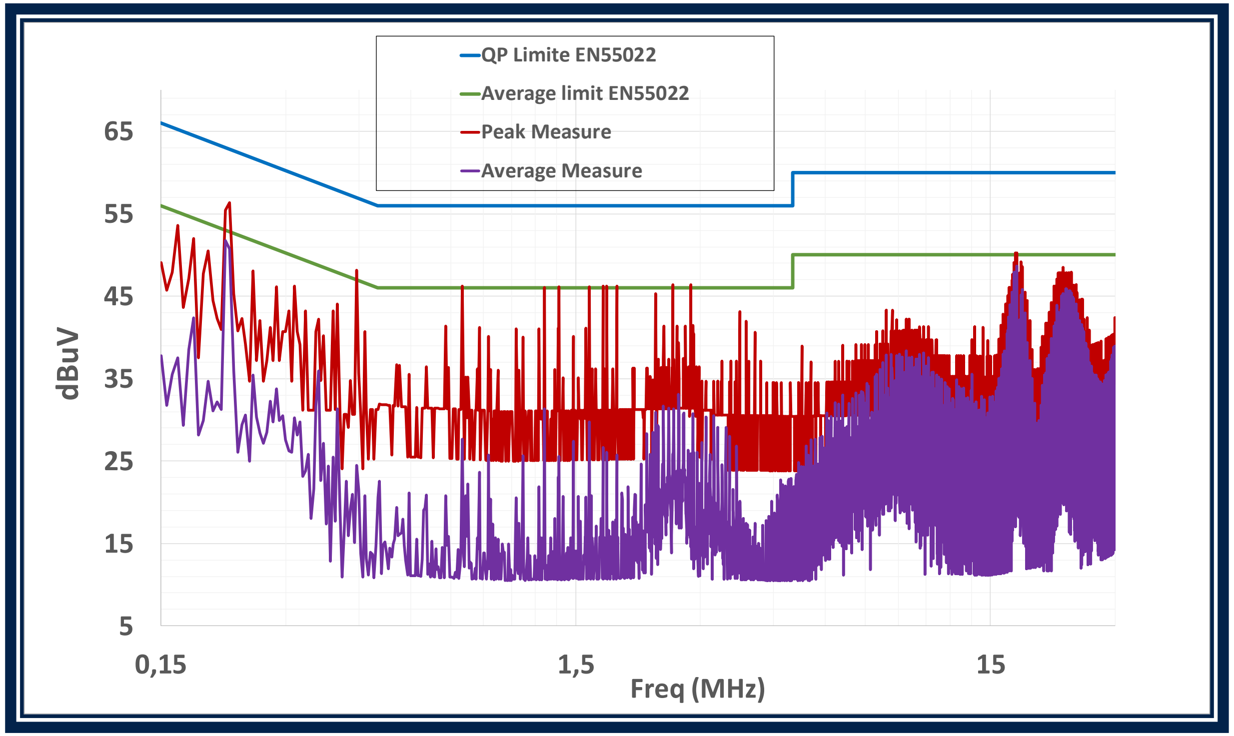
Evaluation board performance
Common mode noise measurement (load = 800 W / 230 V_{RMS} / 50 Hz)

Without smart Duty cycle control



With smart Duty cycle control



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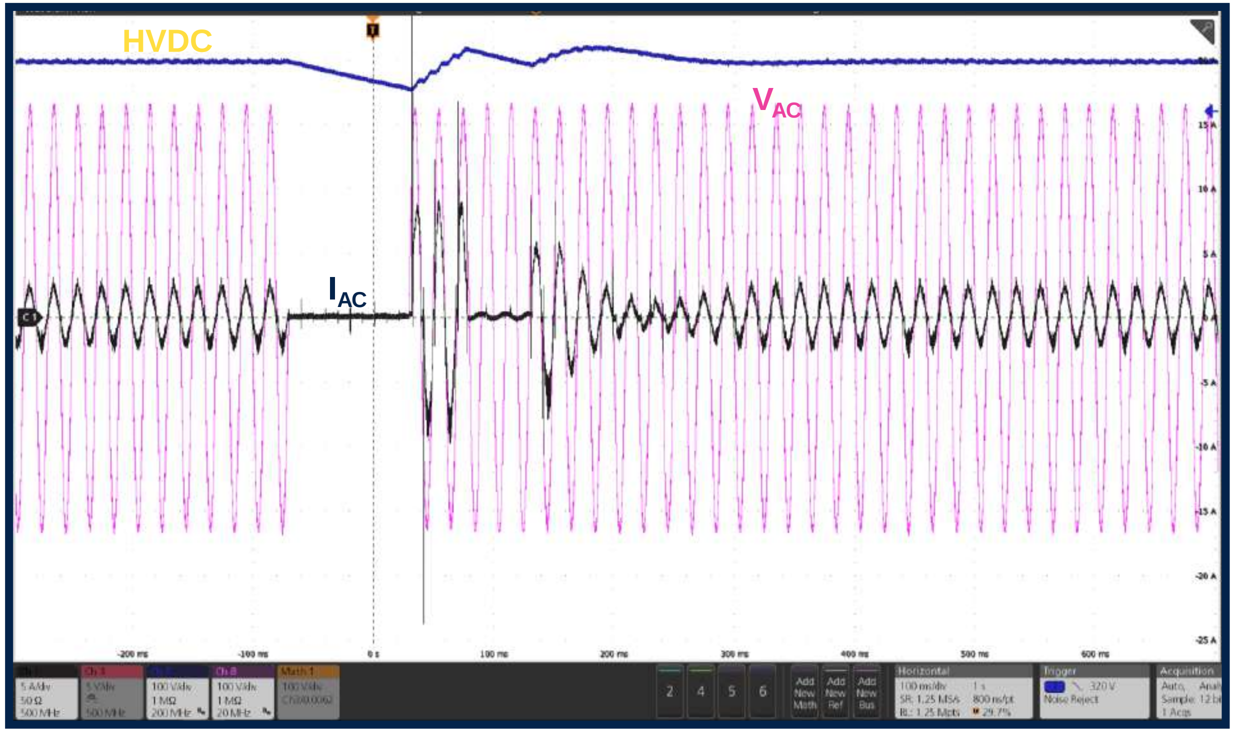
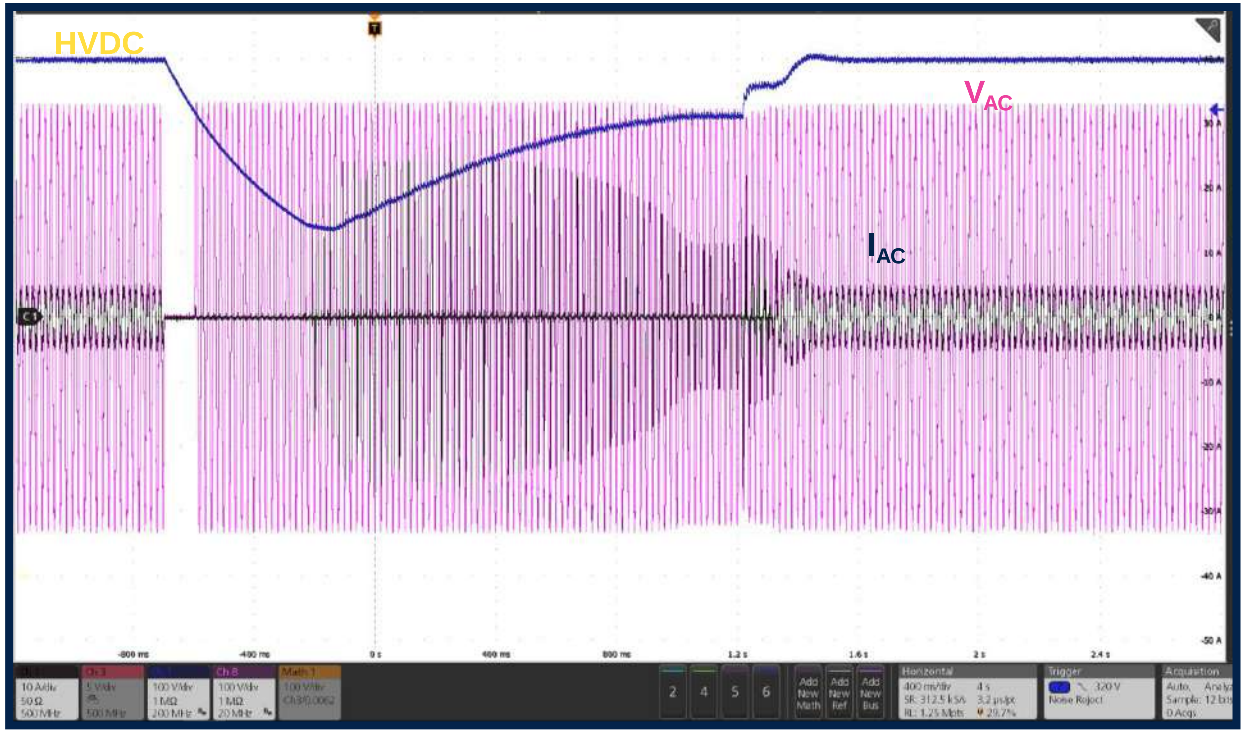
Evaluation board performance
Drop AC line voltage

AC line voltage interrupt lasts less than 30ms
SCRs and SiC MOSFETS are kept “ON”, criteria A



AC line voltage interrupt lasts more than 30ms
SCRs are controlled back in soft-start when the VAC is reapplied, criteria B



With SCRs, AC line voltage interrupt is managed more effectively than NTC + relays solution

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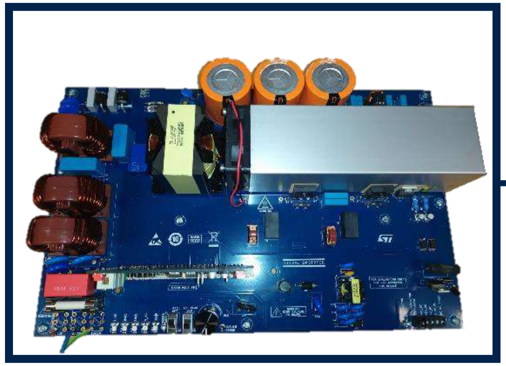
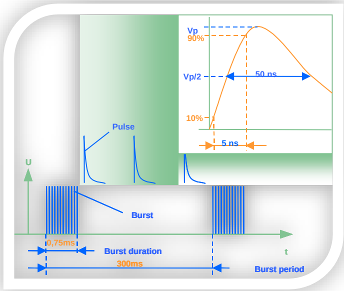
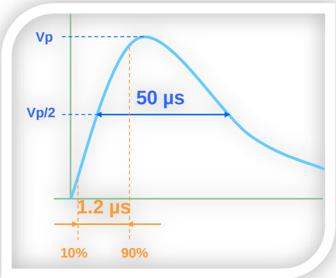
Evaluation board performance
Main figures



- Input AC voltage: 85VAC up to 264VAC
- Input AC frequency: 45Hz up to 65Hz
- DC output voltage: 400VDC
- Switching frequency: 72 kHz
- Maximum input curent: 16 A RMS (POUT = 3.6KW)
- A high efficiency: > 97,5%
- A low THD distortion lower than 5 % of maximum
- Compliant to :
  - **EN 55022 and IEC 61000-4-11 and IEC 61000-3-3**
  - **IEC 61000-4-5 surge: 4kV**
  - **IEC 61000-4-4 EFTY burst : criteria A @ 4kV**
- Cooling: forced air cooling with active fan
- Design for operation with DC/DC converter
- Peak inrush current tuning
- Remove two bulky relays and an NTC resistor thanks to SCRs progressive start-up





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- **Takeaways**

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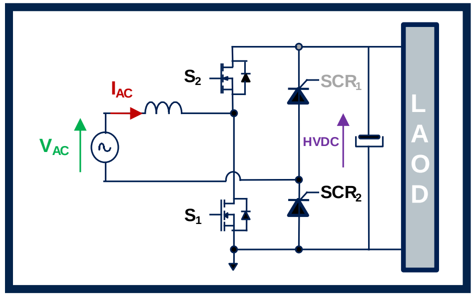
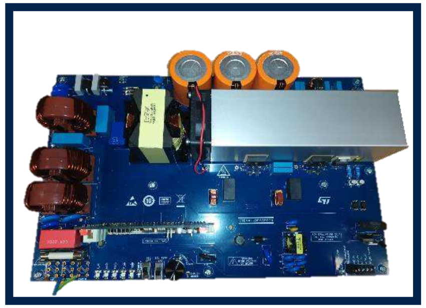
Takeaways

- This presentation described a 3,6kW bridgeless totem pole PFC evaluation board for telecom and industrial applications with an digital Inrush current limiter using SiC MOSFETs and Thyristors.
- The Evaluation board design includes
  - A power board bridgeless totem pole boost with an inrush limiter circuit, SiC MOSFET and SCRs switch drivers and an auxiliary power supply
  - A control board with its MCU, a PFC/ICL control firmware
  - An adapter board for software debug





DC/DC or motor inverter can be connected to this evaluation board

- Evaluate a full ST solution
  - SCRs: To control the inrush-current to charge a DC bus capacitor and to fulfill with the IEC 61000-3-3 standard
  - SiC MOSFETs: To reduce passive components size and to provide a PFC with a very high efficiency thanks to low reverse recovery diode body
  - STGAP2S driver: Dedicated and optimized to control SiC MOSFETs
  - STM32 microcontroller: Embedded the PFC control algorithm

Takeaways

- Check the stand-by losses
  - Reduce drastically the stand-by losses of the traditional NTC/PTC Inrush-current limitation
  - Disconnect the DC bus capacitor from the AC mains when it does not have to operate
  - Without requiring a relay to be added to open the circuit during stand-by
- Check EMC
  - Immunity to fast transient and surge voltages
  - Common mode noise
- This reference design offering:
  - A high efficiency: > 97,5%
  - A low THD distortion lower than 5 % of maximum load
  - A high switching lifetime with reduced EMI emissions
  - A robust circuit that meets EMC standards up to 4 kV
- SCR allows achieving a smart inrush current limitation at power up or line drop recovery compare to the traditional NTC and relays solution

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